AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A system, comprising:

a processor;

a memory coupled to the processor;

a stack that exists in the memory and contains stack data;

a memory controller coupled to the memory; wherein the processor issues data requests; and

wherein the memory controller adjusts memory management policies based on whether the data requests refer to stack data and adjusting the memory management policies includes not allocating the cache line containing stack data within the cache memory, and forwarding the stack data from the secondary memory.

2. (Currently amended) The system of claim 1, wherein the memory comprises a first level of memory and a second level of memory, and wherein the first level of memory is ~~substantially~~ faster than the second level of memory.

3. (Original) The system of claim 2, wherein the first level of memory comprises a cache memory that implements a cache allocation policy, and wherein the cache allocation policy is adjusted based on the type of data access requested.

4. (Currently amended) The system of claim 3, wherein the allocation policy is adjusted when the type of data access refers to stack data that corresponds to a predetermined word in a cache line and the cache line is not present in the cache memory.

5. (Original) The system of claim 4, wherein the type of data request involves writing to the stack.

6. (Original) The system of claim 5, wherein adjusting the memory management policies includes allocating the cache line containing stack data within the cache memory, and updating the stack data within the cache line without fetching data from the secondary memory.

7. (Original) The system of claim 4, wherein the type of data request involves reading from the stack.

8. (Canceled)

9. (Original) The system of claim 4, wherein the predetermined word is the first word in the cache line.

10. (Original) The system of claim 4, wherein the predetermined word is the last word in the cache line.

11. (Currently amended) A method of managing memory, comprising:

issuing a request for data;

indicating whether the requested data is stack data; and

varying the memory management policies depending on whether the requested data is stack data, wherein when the request for data is a read request for stack data

reading data from a main memory without allocating a new cache line within the cache memory, and forwarding the data to the processor.

12. (Original) The method of claim 11, further comprising determining if the requested data corresponds to a predetermined word in a cache line in a cache memory.

13. (Original) The method of claim 12, further comprising determining whether the request for data is a write request or a read request.

14. (Original) The method of claim 13, wherein the request for data is a write request for stack data and the method further comprises writing data to the cache line without fetching data from a main memory.

15. (Original) The method of claim 14, wherein the predetermined word is the first word in the cache line.

16. (Original) The method of claim 14, further comprising enabling a valid bit associated with the cache line.

17. (Canceled)

Please add the following new claim:

18. (New) A system, comprising:

a processor;

a memory coupled to the processor, the memory comprising a cache memory portion and a non-cache memory portion;

a stack that exists in the memory and contains stack data;

a memory controller coupled to the memory; wherein the processor issues data requests; and

wherein the memory controller adjusts an allocation policy associated with the cache memory when a type of data access refers to stack data that corresponds to a predetermined word in a cache line and the cache line is not present in the cache memory.

19. (New) A method of managing memory, comprising:

issuing a request for data;

indicating whether the requested data is stack data; and

adjusting an allocation policy associated with a cache memory when a type of data access refers to stack data that corresponds to a predetermined word in a cache line and the cache line is not present in the cache memory.